

Claims:

- 1 1. A simultaneous multithreaded processor system comprising:
 - 2 a first multiplexer associated to a first thread of instruction pointers; and
 - 3 a second multiplexer associated to a second thread of instruction pointers;
 - 4 said first and second multiplexers to provide instruction pointers for execution in said
 - 5 processor;
 - 6 first and second storage elements coupled to said respective first and second multiplexers,
 - 7 wherein:
 - 8 one of the first and second threads is active while the other of said first and second
 - 9 threads is inactive; and
 - 10 instruction pointers for the active thread are delivered to processor logic and the
 - 11 instruction pointers for the inactive thread are delivered to a storage element for delivery to the
 - 12 processor logic when the inactive thread becomes the active thread.
- 13 2. The system of claim 1, further comprising a common multiplexer coupled between said
- 14 first and second multiplexer and processor logic.
- 15 3. The system of claim 2, wherein the common multiplexer receives instruction pointer data
- 16 sequentially from the first multiplexer and the second multiplexer by utilizing a time-
- 17 multiplexing protocol.
- 18 4. The system of claim 3, wherein the time-multiplexing protocol is a 'round-robin'
- 19 protocol.

1 5. The system of claim 1, wherein the first multiplexer and the second multiplexer are
2 priority multiplexers.

1 6. The system of claim 5, wherein the first multiplexer and the second multiplexer receive
2 instruction pointer information and data from a plurality of stages in a processor pipeline.

1 7. The system of claim 6, wherein the first multiplexer and the second multiplexer receive
2 instruction pointer information and data from re-steer logic at the plurality of stages in the
3 processor pipeline.

8. The system of claim 7, wherein the first multiplexer and the second multiplexer pass the
instruction pointer information and data to the common multiplexer with a pre-determined
priority.

9. The system of claim 1, wherein the storage element is a flip-flop device.

1 10. A method for a simultaneous multithreaded processor system, comprising the steps of:
2 associating a first multiplexer to a first thread of instruction pointers;
3 associating a second multiplexer to a second thread of instruction pointers;
4 providing, by said first and second multiplexers, instruction pointers for execution in
5 said processor;
6 coupling first and second storage elements to said respective first and second
7 multiplexers;

8 establishing one of the first and second threads as active and the other of said first and
9 second threads as inactive;
10 delivering the instruction pointers for the active thread to processor logic; and
11 delivering the instruction pointers for the inactive thread to a storage element for delivery
12 to the processor logic when the inactive thread becomes the active thread.

1 11. The method of claim 10, further comprising:
2 coupling a common multiplexer between said first and second multiplexer and processor
3 logic.

12. The method of claim 11, wherein the common multiplexer receives instruction pointer
data sequentially from the first multiplexer and the second multiplexer by utilizing a time-
multiplexing protocol.

13. The method of claim 12, wherein the time-multiplexing protocol is a 'round-robin'
protocol.

1 14. The method of claim 10, wherein the first multiplexer and the second multiplexer are
2 priority multiplexers.

1 15. The method of claim 14, wherein the first multiplexer and the second multiplexer receive
2 instruction pointer information and data from a plurality of stages in a processor pipeline.

1 16. The method of claim 15, wherein the first multiplexer and the second multiplexer receive
2 instruction pointer information and data from re-steer logic at the plurality of stages in the
3 processor pipeline.

1 17. The method of claim 16, wherein the first multiplexer and the second multiplexer pass
2 the instruction pointer information and data to the common multiplexer with a pre-determined
3 priority.

1 18. The method of claim 10, wherein the storage element is a flip-flop device.

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19. A simultaneous multithreaded processor system comprising:
a first multiplexer associated to a first thread of instruction pointers; and
a second multiplexer associated to a second thread of instruction pointers;
said first and second multiplexers to provide instruction pointers for execution in said
processor;
first and second storage elements coupled to said respective first and second multiplexers,
wherein:
one of the first and second threads is active while the other of said first and second
threads is inactive;
instruction pointers for the active thread are delivered to processor logic and the
instruction pointers for the inactive thread are delivered to a storage element for delivery to the
processor logic when the inactive thread becomes the active thread; and

13 a common multiplexer coupled between said first and second multiplexer and processor
14 logic that receives instruction pointer data sequentially from the first multiplexer and the second
15 multiplexer by utilizing a time-multiplexing protocol.

1 20. The system of claim 19, wherein the first multiplexer and the second multiplexer receive
2 instruction pointer information and data from a plurality of stages in a processor pipeline.

1 21. The system of claim 20, wherein the first multiplexer and the second multiplexer receive
2 instruction pointer information and data from re-steer logic at the plurality of stages in the
3 processor pipeline.

1 22. The system of claim 19, wherein the first multiplexer and the second multiplexer pass the
2 instruction pointer information and data to the common multiplexer with a pre-determined
3 priority.